In the Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a) as failing to show every feature of the invention specified in the claims. Accordingly, Applicants have amended Fig. 2 to include a more complete schematic representation of the system and method claimed herein. A proposed set of drawings is attached as Appendix A to this amendment to overcome the Examiner's objections. Following the Examiner's approval of the form of the proposed drawings, Applicants will submit a formal set of drawings that will comply in all respects with 37 CFR 1.83.

The Examiner also objected to the drawings under 37 CFR 1.83(a) as failing to show every feature of the invention as specified in the claims. Specifically, the examiner objected to the failure to include a "multiplexer" logic function in the drawings, as recited in claim 10. Applicants respectfully submit that the term "multiplexer" is defined in the IBM Dictionary of Computing, McGraw Hill, 1994, compiled and edited by George McDaniel, and is a term readily understood and recognized by a person of ordinary skill in the art. Further, a person of ordinary skill in the art would understand that a multiplexer may be configured to implement a combinatorial logic function, such as an AND gate. Moreover, Applicants' specification at paragraph 0023 indicates that "the combination of the two signals 20 and 22 to generate the effective precharge signal 24 is not restricted to an AND gate, but can also be realized by other logic implementations."

Applicants have amended the drawings to illustrate the memory array components coupled to a logical AND element to produce a precharge control signal based on an external read cycle (n+1) signal and the conventional precharge signal. A set of three replacement sheets are appended to this Reply and Amendment. Accordingly, Applicants respectfully submit that the Examiner's objection to the drawings has been overcome

Remarks

Claims 1-11 are pending in the application and stand rejected. By this amendment claims 1-3 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

Claim Objections

The Examiner objected to claim 3 due to a single quotation mark immediately preceding the term "read cycle (n+1)." Applicants have corrected this typographical error and respectfully submit that the Examiner's objection has been overcome.

Claim Rejections - 35 U.S.C. § 112

The Examiner rejected claims 2, 4, 7 and 10 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner indicated that the term "SRAM" in claim 2 is a relative term which renders the claim indefinite. Applicants respectfully submit that a person of ordinary skill in the art would understand the term SRAM to include that class of integrated circuit memory devices implemented with a standard 6 transistor storage cell configured in an array of m rows by n columns. A person of ordinary skill in the art would similarly classify an SRAM as having a precharge circuit for the bitlines (columns). A person skilled in the art would further recognize that an SRAM does not require a refresh operation because the storage mechanism is not capacitor based. Applicants further submit that a number of seminal electrical engineering texts, including Introduction to VLSI Systems by C. Mead and L. Conway Addison-Wesley, 1980; Microelectronic Circuits by A. Sedra and K. Smith, Oxford University Press, 1982; and Digital Integrated Circuits by Jan Rabaey, Prentice-Hall, 1996, are replete with references to and definitions of SRAM as well as DRAM and other integrated circuit memory arrays.

While functional and structural limitations may be properly recited in a method claim, Applicants have amended claim 1 to refer simply to a "memory array" rather than a "dynamic memory block" to eliminate any inherent ambiguity or contradiction as between claims 1 and 2. Applicants have also amended claim 2 to recite "a memory array comprising a static random access memory (SRAM) array."

The Examiner also rejected claims 4 and 7 as being indefinite due to the relative term "second precharge signal." Applicants respectfully submit that a (first) conventional precharge signal and a (second) precharge control signal are clearly described and illustrated in the specification. (Applicants' specification at paragraphs 11, 12, 22 and 28 and Fig. 2.)

Accordingly, Applicants respectfully submit that the Examiner's rejection of claims 2, 4, 7 and 10 under 35 U.S.C. § 112, second paragraph has been overcome and are therefore in condition for allowance.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent No. 4,926,384 to Roy. The Examiner stated that Roy discloses various elements corresponding to the limitations of Applicants' independent claim 1, citing Col. 3, lines 12-25. Applicants respectfully submit that Roy is directed to a method of improving write cycle recovery time by automatically equalizing bitline voltages at the end of a write cycle, instead of the beginning of a read cycle. (Roy, Col. 2, lines 42-46.) Roy discloses a memory and associated method for improving memory access latency, i.e. performance, by removing the process of equalizing the bitlines from the critical timing path. (Col. 3, lines 19-28), whereas Applicants' method is directed to reducing power dissipation from unnecessary charging of memory bitlines following a write access. In other words, Applicants' method contemplates precharging the bitlines of the memory only when a read access follows the current access operation. (Applicants' Specification at paragraph 11, claim 1.) When a write access follows the current access operation, Applicants'

precharge circuitry is disabled. (Applicants' Specification at paragraph 11, claim 1.) Conversely, Roy teaches a method wherein the bitlines are equalized at the conclusion of each write cycle regardless of whether the following access will be a read operation. Moreover, a bitline equalization process is different from an active precharge operation because the bitlines are settling to an average potential between the true and complement values to avoid a full-swing transition rather than being charged to a rail potential. (Roy at Col. 3, lines 5-10 and Col. 10, lines 61-65.) More importantly, the bitline equalization process of Roy occurs at the end of **each** write cycle and only in the memory block to which data has been written. (Roy at Col. 3, lines 21-23.) The scheduling of Applicants' bitline precharge operation therefore occurs at a different time in the memory access cycle, namely only when the next cycle will perform a read access operation. Further, the bitline operation contemplated by Applicants' herein is an active precharge rather than a passive equalization.

The Examiner rejected claims 7(8)-11 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent No. 4,926,384 to Roy. As noted above, Applicants' invention is based on a different timing sequence for precharge as well as different precharge mechanism, namely bitline equalization versus full bitline precharge. Similarly, Roy does not disclose nor claim a memory array having a read cycle signal controller for generating a read cycle (n+1) signal when a next memory access operation is a read access operation, nor does Roy evaluate the first precharge control signal and the read cycle control (n+1) signal to determine whether a next memory access is a read access operation for gating the precharge circuit. (Applicants' Specification, paragraphs 11-13, claim 8.)

In addition, Applicants' describe a mode of operation in which the latency required to evaluate whether the n+1 cycle will be a read access is generated by adding an extra clock cycle to the memory access time. (Applicants' Specification at paragraph 30, claim 7.) As such, the methodology claimed by Applicants emphasizes the stated objective of saving power at the expense of performance, which is similarly not anticipated by Roy.

A claim is anticipated only if each and every element as set forth in the claim is found,

either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Roy does not teach the element of disabling a precharge operation when data are written in the next memory access cycle nor of incurring a memory performance penalty to reduce power dissipation associated with bitline precharge operations. Therefore Roy does not anticipate every element of Applicants' claimed method and memory array. Claims 2-7 and 12 depend from claim 1 as amended. Claims 9-11 depend from claim 8. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 1-11 under 35 U.S.C. § 102(b) has been overcome.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Chiang, et al. (U.S. Patent No. 5,950,223); Freyman, et al. (U.S. Patent No. 5,745,427); and Van de Graff et al. (U.S. Patent No. 6,141,272, have been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claim 1 and independent claim 8.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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Appendix A

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